

# Adaptive Nonlinear Cancellation for High-Speed Fiber-Optic Systems

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**Abstract**—In this paper, we propose techniques for adaptive nonlinear cancellation of intersymbol interference in the electrical signal at the receiver in Gb/s lightwave systems, and describe several demonstrations of these techniques. We first discuss techniques for adjustable nonlinear cancellation, and describe demonstrations of these techniques using commercially available integrated circuits (IC's) at data rates as high as 1.7 Gb/s. We then discuss techniques for automatic adjustment and describe a demonstration of adaptive nonlinear cancellation at 450 Mb/s. Our experimental results show that these techniques allow reliable detection even when the received signal eye is closed by intersymbol interference, such as from polarization or chromatic dispersion. Finally, we discuss how these techniques can be integrated onto the detector IC for operation at 2.5 Gb/s and higher data rates. These techniques allow a single IC detector with adaptive nonlinear cancellation to be used in long-haul and undersea lightwave systems to optimize the detector threshold and compensate for the ISI due to such impairments as polarization and chromatic dispersion, nonideal receiver frequency characteristics, and transmitter/receiver mismatch.

## I. INTRODUCTION

**S**IGNAL dispersion is a major factor limiting the maximum distance and/or bit rate of long-haul fiber-optic systems, but the effect of this dispersion and its limitations can be reduced by signal processing of the electrical signal at the receiver. However, to be practical, the signal processing must be adaptive, since the dispersion can vary with time, yet it must also operate at the Gb/s data rate of these systems.

Previous papers [1]–[9] have described electrical signal processing techniques at the receiver, methods for implementing these techniques at high data rates, and their reduction in the effects of signal dispersion or intersymbol interference (ISI). The signal processing techniques include linear equalization [1]–[7], nonlinear cancellation [1], [8], and maximum likelihood detection [1], [9]. Linear equalization, which can compensate only linear distortion, has been demonstrated using microstrip lines at 4 Gb/s to compensate for chromatic dispersion in coherent detection systems [4], and using analog tapped delay lines at 1.4 Gb/s to compensate for polarization dispersion [6] and at 8 Gb/s to compensate for nonideal receiver response [2]. However, when the distortion is severe, such as with large polarization dispersion, or when the distortion is nonlinear, such as with chromatic dispersion with direct detection, nonlinear techniques, such as nonlinear cancellation, are required. Nonlinear cancellation has the additional advantage that it can be integrated onto the detector integrated circuit

(IC) [8], whereas the linear equalization techniques described above cannot. However, nonlinear cancellation has not been previously demonstrated at high data rates, although methods for implementation of nonlinear cancellation at high data rates have been previously described [8].

To be practical in high data rate fiber-optic systems, signal processing must also be adaptive. Polarization dispersion varies with time [10]–[12], changing at a rate on the order of seconds to hours, while nonideal receiver response varies among receivers and transmitter/receiver pairs and also changes with aging. Signal distortion due to chromatic dispersion in direct detection systems varies with the chirp of the transmit laser, which also varies among lasers. Although in coherent detection systems the signal distortion due to chromatic dispersion [13] in a given fiber is constant, the distortion varies with the fiber length. Furthermore, in future high-speed fiber-optic systems, all three impairments—nonideal receiver response, and polarization and chromatic dispersion—may have a significant effect on the ISI. Thus, adaptive signal processing is required to track these impairments and to allow automatic startup. The linear equalizers that have been demonstrated in high-speed fiber-optic systems [2], [4], [6] were not adaptive, however, and, although adaptive techniques for linear equalizers have been described [1], none have been demonstrated at high data rates. Adaptive techniques for high-speed nonlinear cancellation have not been previously proposed or demonstrated.

In this paper, we propose techniques for adaptive nonlinear cancellation of intersymbol interference in the electrical signal at the receiver in Gb/s lightwave systems, and describe several demonstrations of these techniques. We first discuss techniques for adjustable nonlinear cancellation, and describe three demonstrations of these techniques using commercially available IC's at data rates as high as 1.7 Gb/s. We then discuss techniques for automatic adjustment and describe a demonstration of adaptive nonlinear cancellation at 450 Mb/s. Our experimental results show that these techniques allow reliable detection even when the received signal eye is closed by intersymbol interference, such as from polarization or chromatic dispersion. Finally, we discuss how these techniques can be integrated onto the detector IC for operation at 2.5 Gb/s and higher data rates.

In Section II, we describe techniques and demonstrations of nonlinear cancellation using commercially available IC's. Techniques and a demonstration of adaptive nonlinear cancellation are described in Section III. In Section IV, we discuss the application of these techniques on IC's for operation at

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Gb/s data rates. A summary and conclusions are presented in Section V.

## II. NONLINEAR CANCELLATION

Consider a received signal distorted by ISI from previous bits. This distortion could be caused by, e.g., nonideal receiver or transmitter frequency response, chromatic dispersion, or polarization dispersion, all of which cause components of the transmitted signal to arrive at the receiver with different amplitudes and delays. Since these components depend on the transmitted bit pattern, the resulting distorted signal has both level-transition timing and amplitude near the center of the eye that varies with the bit pattern. Thus, the ISI can cause the received signal eye opening to become smaller in the horizontal (time) as well as the vertical (amplitude) direction. In this paper, we will focus primarily on the compensation of the amplitude distortion near the center of the eye, although pattern-dependent distortion in the horizontal direction can also be compensated by the nonlinear cancellation techniques described in this paper, as shown later.

With amplitude distortion, at time  $t_k$  at the center of the received signal eye, the electrical signal is given by

$$s_k = x_k + f(x_{k-1}, x_{k-2}, \dots) \quad (1)$$

where  $x_k$  is the transmitted signal (0,1), and  $f(\cdot)$  is a given function of the previous bits. In many systems, the ISI from the previous bit dominates over the ISI from other previous bits. Therefore, for simplicity in the examples discussed in this paper and in our experiment, we consider ISI due to the previous bit only, i.e.,

$$s_k = x_k + \alpha x_{k-1} \quad (2)$$

where  $0 \leq \alpha \leq 1$ . Since in many receivers automatic gain control is used to keep the peak signal level constant, let us normalize  $s_k$  by its peak value of  $1 + \alpha$  to obtain

$$s_k = (x_k + \alpha x_{k-1}) / (1 + \alpha). \quad (3)$$

Thus,  $s_k$  can take on the values of 0,  $\alpha/(1 + \alpha)$ ,  $1/(1 + \alpha)$  and 1 when  $(x_{k-1} x_k)$  is (0 0), (1 0), (0 1), and (1 1), respectively. Fig. 1 shows the received signal eye near the sampling time for  $\alpha \approx 0.9$  without noise or other ISI. In this figure, the signal levels for the above four cases are labeled.

To detect the received bit, the received signal at time  $t_k$  is compared to a threshold level. In a standard detector, the threshold level is fixed, and, for ISI from the previous bit (3), the optimum threshold  $TH_f$  is 1/2. Fig. 1 shows that with this threshold the minimum eye opening is only  $1 - \frac{2\alpha}{1+\alpha}$ , and the detected bits are easily corrupted by noise or other signal distortion. The nonlinear canceler [1], [8], however, changes the threshold level to  $TH_0\left(\frac{1}{2} - \frac{\alpha}{2+2\alpha}\right)$  or  $TH_1\left(\frac{1}{2} + \frac{\alpha}{2+2\alpha}\right)$  if the previous bit is a 0 or 1, respectively. As shown in Fig. 1, this increases the difference in signal levels for 1's and 0's from  $1 - \frac{2\alpha}{1+\alpha}$  to  $1 - \frac{\alpha}{1+\alpha}$ . Note that, even if the received signal eye is closed due to ISI the one-bit nonlinear canceler can reliably detect the signal.

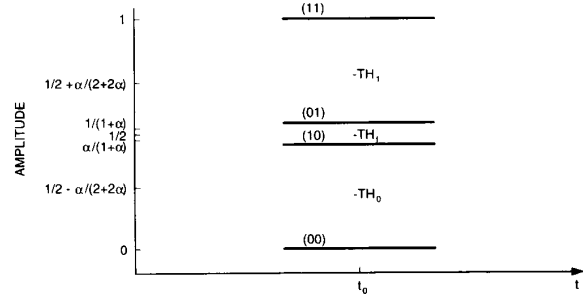


Fig. 1. Sketch of the received signal eye for  $\alpha \approx 0.9$ , showing the signal levels at the sampling time for the four two-bit patterns (with the signal level transitions not shown).

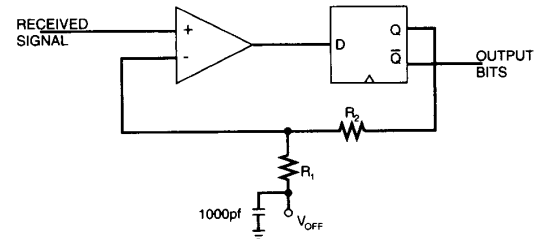


Fig. 2. Block diagram of a one-bit nonlinear canceler using analog feedback.

Fig. 2 shows one method for implementing the one-bit nonlinear canceler. The output of a standard detector, which consists of a comparator followed by a flip-flop, is fed back to the threshold of the comparator through a voltage divider. Thus, an output bit of 1 increases, while a 0 decreases, the threshold level about an offset level  $V_{off}$ , by an amount that depends on the ratio of the voltage divider resistors  $R_1/R_2$ .

To experimentally demonstrate this technique, we considered four high-speed detectors: the AT&T LG1088AX (which has a maximum data rate of 1.7 Gb/s), the GigaBit Logic 10G021A (2.7 Gb/s), the Sony CXB1107Q (2.3 Gb/s), and the NEC UPG706B-1 (4.0 Gb/s). The NEC UPG706B-1 is actually a high sensitivity (200 mV) flip-flop, but can be considered as a low sensitivity detector since the other detectors have sensitivities of about 50 mV.

The maximum data rate of the nonlinear canceler is limited to less than the above values by the propagation delay of the feedback path and the detector. With these single IC detectors, the delay of the feedback path can be kept below 100 ps. However, the propagation delay of these detectors varies widely: 1200 ps was measured for the AT&T and GigaBit Logic detectors, 570 ps is specified for the Sony detector, and 400 ps was measured for the NEC detector. The lower delay of the NEC detector can be attributed to fewer stages in the detector, which causes the loss of sensitivity. Thus, the maximum data rate for the nonlinear canceler using these detectors ranges from about 800 Mb/s for the AT&T and GigaBit Logic detectors, to about 2 Gb/s for the NEC detector. Below we describe demonstrations of nonlinear cancellation using the GigaBit Logic and NEC detectors.

Fig. 3 shows the experimental setup used to demonstrate one-bit nonlinear cancellation using the GigaBit Logic and

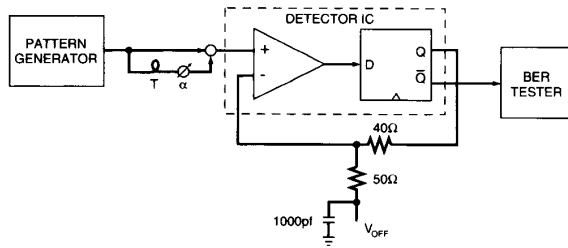


Fig. 3. Block diagram of the experimental setup used to demonstrate one-bit nonlinear cancellation with analog feedback.

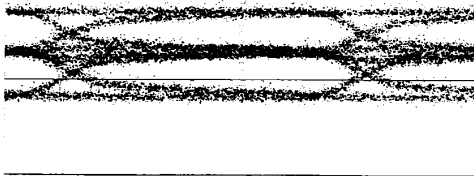


Fig. 4. The received signal eye with ISI in the analog feedback, one-bit nonlinear canceler experiment.

NEC detectors. To generate the ISI to be canceled, a two-tap, analog tapped delay line was used. The output of the signal generator was split two ways: one signal was delayed by one bit period, attenuated, and combined with the other signal. In the experiment, the delayed signal was attenuated 1 dB in power, and thus the resulting signal is given by (2) with  $\alpha \approx 0.9$ .

Fig. 4 shows the resulting eye with ISI. Note that there are four distinct levels at the sampling time or center of the eye, corresponding to (0 0), (0 1), (1 0), and (1 1), although the middle two levels are too close to be separated. Eight distinct transitions in the eye can be seen, corresponding to the eight possible transitions between the four two-bit patterns. Note also that the eye is closed, although without noise and with perfect signals, the eye would be slightly open.

With the signal distorted by the tapped delay line, the bit error rate with a standard detector was 0.5 for the attenuator at 1 dB, corresponding to a signal to ISI power ratio  $S/I$  of 1 dB. The bit error rate was less than  $10^{-9}$  only for  $S/I \geq 7$  dB. However, with the one-bit nonlinear canceler, the bit error rate was measured at less than  $10^{-9}$  for  $S/I = 1$  dB for the 10G021A at 800 Mb/s and the UPG706B-1 at 1.7 Gb/s. The UPG706B-1 may have been capable of operating up to 2 Gb/s, but 1.7 Gb/s was used in order to demonstrate nonlinear cancellation at the data rate of FT series G.

The performance of the nonlinear canceler was degraded somewhat by distortion in the feedback signal. Fig. 5 shows the eye of the feedback signal with the 10G021A—the overshoot of the feedback signal for a (0 1) pattern is evident. This distortion caused the detector to be more sensitive to noise, but did not significantly affect our experiment because the noise level was low.

An additional point to note for this canceler is that it is

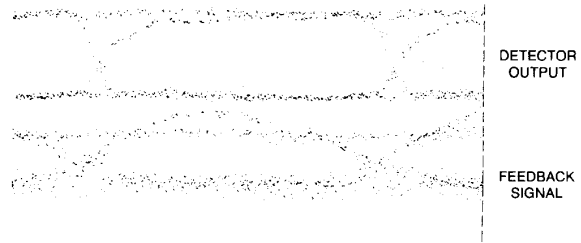


Fig. 5. The eye of the feedback signal in the analog feedback, one-bit nonlinear canceler experiment using the 10G021A.

difficult to determine the values of  $R_1$ ,  $R_2$ , and  $V_{off}$  that give the necessary threshold levels  $TH_0$  and  $TH_1$ , because these levels also depend on the threshold detector input and output characteristics, such as impedance and bias current. To avoid this problem, in the experiment we adjusted the distorted signal to match the canceler. This is, of course, opposite of what should be done in practical systems, where it is desirable, at the very least, to be able to manually adjust the threshold levels to match the ISI. To manually adjust the threshold levels with this implementation, both  $V_{off}$  and the resistor values must be adjustable. Unfortunately, at Gb/s speeds, variable passive resistors (potentiometers) are not practical. One alternative is to use a fixed value for  $R_2$  but use a series of smaller resistors to implement  $R_1$ , with wires used to bypass these smaller resistors. The value of  $R_1$  can then be manually adjusted by successively removing these wires, although this can only be done once. This technique was implemented on a HIC by M.J. Badcock and J. Nagel and demonstrated at 1.7 Gb/s using the UPG706B-1 detector. Furthermore, for electronically adjustable thresholds, variable gain GaAs FET attenuators can be used [14]. Commercially available devices operate with bandwidths up to 18 GHz [15].

The above problems of analog feedback in the nonlinear canceler—data rate limitation due to propagation delay, and distorted and difficult to calculate threshold levels—can be avoided by using multiple detectors with different fixed threshold levels, rather than one detector with varying threshold levels. The output bits are obtained by selecting the output of the detector with the threshold that corresponds to the previously detected bits, as discussed in [8]. For a one-bit nonlinear canceler, two detectors plus a 2:1 multiplexer are required to implement this technique, as shown in Fig. 6. Note that the threshold levels are directly accessible and fixed without the problems of analog feedback, and the data rate is limited only by the propagation delay of the multiplexer—a limitation that can be overcome by using look-ahead logic [8]. This multiple-detector implementation also has the advantages that it is easier to extend to multiple-bit nonlinear cancellation than the analog feedback technique, and can have different sampling times for different bit patterns to compensate for pattern-dependent timing distortion. However, in our experiment we implemented only a one-bit canceler with identical sampling times for both detectors.

This nonlinear canceler was implemented using two GigaBit Logic detectors (10G021A, as before) and multiplexer 10G023. The maximum data rate was limited to 900 Mb/s

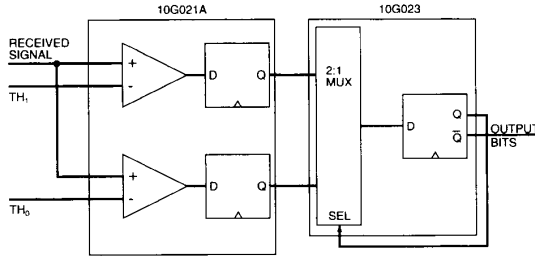


Fig. 6. Block diagram of a one-bit nonlinear canceler using multiple detectors.

by the propagation delay of the multiplexer. Note that, as mentioned above, look-ahead logic could be used to increase the maximum data rate to 2.7 Gb/s, but this would require additional IC's. Using the same experimental setup as before (Fig. 3), we demonstrated that the bit error rate with this nonlinear canceler was less than  $10^{-9}$  with  $S/I = 1$  dB. Furthermore, since the threshold levels were directly accessible, we were able to adjust the threshold levels to demonstrate an error of less than  $10^{-9}$  for all values of  $S/I \leq 0$  dB.

### III. ADAPTIVE NONLINEAR CANCELLATION

Let us now consider techniques for automatic electronic adjustment of the threshold levels in the nonlinear canceler. As discussed above, both the analog feedback and multiple detector implementations of the nonlinear canceler can be electronically adjusted. However, we will only consider adaptive techniques for the multiple detector implementation because of this implementation's advantages.

We can consider the threshold calculation problem for each detector in the multiple detector implementation to be the same as that for a standard detector, but with the received signal used for threshold calculation of a given detector only when the corresponding bit pattern is detected. Therefore, let us first consider two previously published techniques for threshold calculation for a standard detector. One technique is quantized feedback, which can be used to adjust the threshold to compensate for dc offset drifts over many bits, and has been demonstrated at 1 Gb/s [16]. However, this technique requires the offset to be known *a priori*, and therefore is not applicable to our adaptive problem. A second technique is to vary the threshold of a second detector and use the error rate of this detector, as compared to the output of the main detector (assuming the main detector has a lower error rate), to determine the eye opening and, thus, the optimum threshold level [17].<sup>1</sup> Although this technique can be used to track the optimum threshold level, it has the following disadvantages for our nonlinear canceler. First, the requirement of a low

<sup>1</sup> A similar technique was proposed [17] to determine the optimum sampling time also. Here, we will not consider the calculation of the optimum sampling time, but assume that external circuitry is used for timing recovery. With severe ISI, where conventional timing recovery techniques may fail, separate timing recovery loops can be used for each of the detectors, and the nonlinear canceler can then also compensate for pattern-dependent timing distortion. The performance of different sampling times for each detector (pattern-dependent sampling time) is a topic of further research. In our experiment, the sampling time was fixed (and equal) for both detectors at the optimum sampling time without ISI.

error rate with the main detector may not always hold during the initial acquisition of the threshold. This problem is further compounded in the nonlinear canceler because errors in the main detector will cause the threshold of the wrong detector to be adjusted. Second, the technique requires a control IC in addition to the detector IC, while we prefer to have the adaptive circuitry incorporated onto the same IC as the nonlinear canceler (see Section IV).

Here we propose the following adaptive threshold technique. Each threshold is determined by averaging, for a given sequence of previously detected bits, the estimated signal level for a current bit of 0 with that for a current bit of 1. Thus, for a one-bit nonlinear canceler, referring to Fig. 1,  $TH_0$  is the average of the signal levels at  $t_k$  for (0 0) and (0 1), and  $TH_1$  is the average of the signal levels at  $t_k$  for (1 0) and (1 1). The estimated signal level for a given bit sequence (current bit plus previously detected bits) is determined by a detector whose output is enabled only when the given bit sequence is detected and whose threshold level is adjusted, using feedback from the detector output, to be approximately equal to the signal level during that bit period.

This technique was implemented for the one-bit nonlinear canceler using GigaBit Logic GaAs IC's. Fig. 7 shows a block diagram of this adaptive nonlinear canceler. Note that we have added four detectors and a demultiplexer to the nonlinear canceler of Fig. 6. These detectors, 16G061's, are pin drivers whose output is tristated (enabled or disabled) by a control signal from the demultiplexer, which enables the output of the detector in each bit period that corresponds to the detected bit sequence. The signal into the 16G061's is delayed relative to the signal into the main detectors (10G021A), such that the control signal for a given bit pattern is synchronized with the occurrence of that bit pattern in the received signal at the 16G061's. The output of each 16G061 detector is low-pass filtered and fed back to the detector's threshold. With this feedback loop, the threshold level into the 16G061 will be adjusted until it is approximately (see below) at the signal level for the corresponding bit sequence. Specifically, if the threshold level is below the signal level, the 16G061 detector output will be 1 and the threshold level will increase, while similarly the threshold level will decrease if it is above the signal level. The threshold levels of each pair of 16G061 detectors are averaged using a resistive voltage divider, and this averaged level is used as the threshold level in the appropriate main detector (10G021A).

Several issues were considered in the design of this circuitry. First, the resistor values of  $R_1$  and  $R_2$  had to be less than 1 k $\Omega$  so that the small currents into the thresholds of the 16G061 and 10G021A detectors did not produce significant voltage drops across these resistors. However, with these resistance values, the voltage divider affected the low-pass filter, and, therefore, an operational amplifier (LF347) configured as a dc voltage follower was used. Note that the op-amp only needed to operate at the adaptation speed of the circuitry, not at Gb/s data rates. The adaptation speed is determined by the values of  $R_1$  and  $C$ , i.e., the low-pass filter with 3 dB bandwidth  $f_{3\text{ dB}} = \frac{1}{2\pi R_1 C}$ . This speed has to be fast enough to track the impairments and allow for rapid startup,

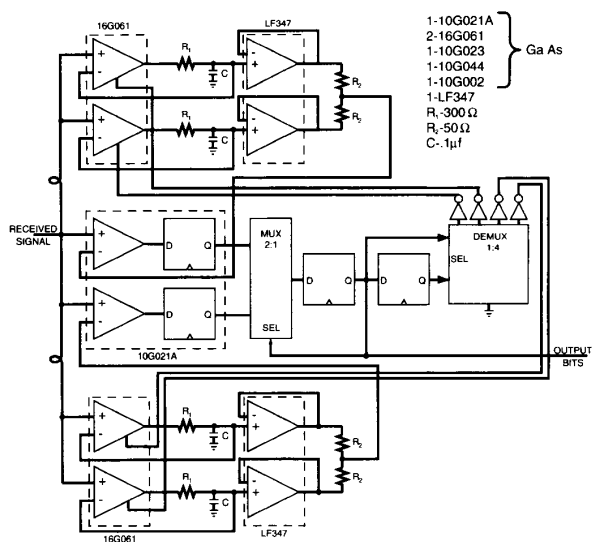


Fig. 7. Block diagram of an adaptive one-bit nonlinear canceler using multiple detectors.

yet must be slow enough to reduce noise effects and keep the threshold level, which is determined the voltage across a capacitor, reasonably constant between occurrences of the corresponding bit patterns. Fortunately, any speed between 10 Hz and 10 MHz easily meets the above requirements. In our experiment, we chose a value in the middle of this range  $f \approx 5$  kHz.

A key issue is how the 16G061 detectors, with the feedback loop, acquire and track the signal level, i.e., the 16G061 threshold level. The 16G061 outputs a high level when the signal level is above the threshold level and a low level otherwise, with these levels determined by external voltage sources. In the experiment, these levels were set at 0 and -2 V so that they were outside the range of the ECL level (typically -0.7 to -1.8 V) input signals and thus all input signal levels could be tracked. This range of levels should also be adequate for many applications since, typically, the input signal amplitude is controlled by an AGC amplifier and AC coupled into the detector. In the experiment, a bias tee was used to adjust the input signal to between 0 and -2 V. Thus, to produce a 16G061 threshold level of  $-\beta$  (0 to -2 V), the comparator must output 1's with probability  $\frac{\beta+2}{2}$  and output 0's with probability  $\beta/2$ . Therefore, in tracking a signal level ( $-\beta$ ) for a given bit pattern, the threshold will be approximately at the level that the signal exceeds with probability  $1 - \beta/2$ . The threshold is, therefore, at the median signal level when the signal level is around -1 V, but is skewed towards -1 V when the signal level deviates from -1 V. Fig. 8 shows an example of this effect. For a given range of input signal levels, this skewing can be reduced, i.e., the threshold will approach the median signal level, if the range of 16G061 output high and low levels is increased. However, 0 and -2 V worked adequately in our experiment.

As compared to determining the mean signal level, this method has the advantages that 1) the skewing, which can



Fig. 8. The received signal eye with ISI showing the estimated signal levels with skewing.

be controlled by adjusting the output levels, tends to ignore large signal deviations and places the thresholds more toward the center of the eye, and 2) the median signal level is less sensitive to large signal deviations caused by bit errors in the main detector.

Now let us consider acquisition of the signal levels. First, we note that acquisition of the signal levels may not occur if the signal is always higher or lower than the threshold level in the main (10G021A) detector. In that case, since the 10G021A output bits are always the same, one of the pair of 16G061 detectors used to determine the 10G021A threshold is never enabled, and the threshold may never be properly adjusted. However, this problem can be avoided at startup by setting the initial levels (thresholds) at -2 V or at the dc level since the input is ac coupled. Furthermore, this problem should not occur during tracking since the ISI should not change abruptly.

If the signal does cross the threshold, though, then acquisition can occur. Consider the acquisition of  $TH_0$ , when the median received signal levels are  $\beta_0$  and  $\beta_1$  for bit patterns (0 0) and (0 1). As long as the error rate for (0 0) is less than  $1 - \beta_0/2$ , the 16G061 threshold level for (0 0) will be adjusted to within the (0 0) received signal level. Similarly, the 16G061 threshold level for (0 1) will be adjusted to within the (0 1) received signal level as long as the error rate for (0 1) is less than  $\beta_1/2$ . Thus, the average of the (0 0) and (0 1) signal levels,  $TH_0$ , will be adjusted close to the correct level. This decreases the bit error rate and thereby further increases the accuracy of the (0 0) and (0 1) signal levels. Thus, all levels will be adapted to their correct levels as long as the initial bit error rate is low enough. This required bit error rate can be reduced to approximately 0.5 by increasing the range of the high and low levels out of the 16G061. Thus, this adaptive technique can acquire and track the thresholds under almost all conditions.

The adaptive nonlinear cancellation technique was demonstrated at 450 Mb/s. The bit error rate was less than  $10^{-9}$  over all values of ISI from the previous bit ( $S/I \geq 0$  dB) and signal level offset, as long as the signal was between -0 to -2 V and the optimum threshold between -0.3 and -1.8 V. A short burst ( $<100 \mu s$ ) of errors occurred when the attenuator in the tapped delay line was manually switched between attenuation values showing that rapid acquisition occurred even with abrupt changes in ISI.

In the experiment, the received signal levels were acquired and tracked up to 900 Mb/s, which is the limit for the manually adjustable nonlinear canceler. However, as the data

rate was increased from 450 to 900 Mb/s, the sensitivity of the 16G061 decreased, while the additional signal distortion caused by the circuitry increased. Thus, at 900 Mb/s, we could not obtain a less than  $10^{-9}$  bit error rate for all  $S/I$ . The problem could have been eliminated, at the expense of two additional IC's, by using 10G021A's as the signal level comparators, followed by the 16G061's to tristate the outputs, in place of the 16G061's alone.

#### IV. APPLICATIONS TO SINGLE IC'S

One of the main goals of this work was to devise and demonstrate techniques for adaptive nonlinear cancellation that can be integrated onto a single IC. This integration has two main advantages. First, integration of nonlinear cancellation on the detector IC permits higher data rates. In the analog feedback nonlinear cancellation demonstrations, the data rate was limited by the propagation delay of the feedback path and the device. With integration, the delay of the feedback path becomes negligible. Furthermore, since most of the propagation delay of the device is due to buffers and drivers for IC signal input and output, with integration, these delays are eliminated. Thus, with integration, the analog feedback nonlinear canceler may operate with only a 30% data rate decrease as compared to a standard detector [8]. Thus, an analog feedback nonlinear canceler may be practical at data rates of 2.5 Gb/s and higher. In the multiple detector nonlinear cancellation demonstration, the data rate was limited by the propagation delay of the feedback path and the multiplexer. Again, with integration, both these delays are greatly reduced—a GigaBit Logic multiplexer with integrated feedback (using a SC100000 GaAs Standard Cell Array) should operate at 2.5 Gb/s [18]. If the delay is too large, however, as discussed before look-ahead computation can be used to eliminate the feedback delay problem and operate the nonlinear canceler at the maximum data rate of the detector [8]. This is achieved at the expense of additional logic, but this logic can be easily incorporated onto the detector IC.

A second advantage of integration is that, since the adaptive nonlinear canceler requires the same inputs as a standard detector (the received signal and clock), adaptive nonlinear cancellation can be incorporated onto the detector IC, with pin-for-pin compatibility with existing detectors. Thus, adaptive nonlinear cancellation would be transparent to the user, i.e., the IC could be considered by the user as merely a higher performance detector that is robust against ISI and automatically adjusts the threshold to the optimum level even without ISI. All the components of the adaptive circuitry—flip-flops, comparators, tristate buffers, demultiplexers, and dc voltage followers—can be easily incorporated onto the detector IC for operation up to the maximum speed of the detector. The main additional issue that must be considered, however, is the delay of the signal into the adaptive circuitry. As seen in Fig. 7, the signal into the adaptive circuitry must be delayed several bit intervals, i.e., the delay of the detector, multiplexer, flip-flop, and demultiplexer. In the demonstration, this delay was obtained by using a longer cable to the input of the adaptive circuitry, with the length of this cable dependent on the bit

rate. For pin-for-pin compatibility with bit rate independent operation, this delay must be incorporated onto the IC. This can be achieved by using additional flip-flops between the signal level comparators and the tristate buffers. Note that for bit rate independent operation, the control signals into the tristate buffers may also need to be clocked (for synchronous operation), which would require an additional flip-flop for each control signal.

For a one-bit nonlinear canceler, the adaptive circuitry, even with the added flip-flops for delay, can be easily incorporated onto a single IC. However, with an  $N$ -bit nonlinear canceler, the number of signal level detectors and the size of the demultiplexer is  $2^{N+1}$ , and the number of flip-flops for delay is proportional to  $N \cdot 2^{N+1}$ . Thus, as  $N$  increases, it may no longer be feasible to incorporate all the adaptive circuitry onto a single IC. However, the circuit complexity can be greatly reduced by time sharing a single signal level detector loop, which includes the comparator, tristate buffer, and low-pass filter connected with feedback. This requires an additional controller IC, and pin-for-pin compatibility may no longer be possible. However, since the minimum adaptation speed for tracking impairments ( $<10$  Hz) is so much lower than the data rate, large  $N$  can be handled by a single loop with  $2^{N+1}$  time sharing. Consider the following example for an  $N$ -bit adaptive nonlinear canceler. Assume that each bit pattern is equally likely to be transmitted, i.e., a given pattern occurs with probability  $2^{-(N+1)}$ . If 100 occurrences of these patterns can generate an accurate signal level,  $100 \cdot 2^{N+1}$  bits are required to estimate a given signal level, and  $100 \cdot 2^{2N+2}$  bits are required to estimate all signal levels and thresholds. If accurate tracking of the signal levels can be obtained by updating the threshold levels at 100 times the maximum speed of ISI variations, then, with a 10 Hz adaptation speed, the data rate must be greater than  $10^5 \cdot 2^{2N+1}$  bits/second for adaptation with a single, time-shared loop. Thus, a single loop can be used to adapt a six-bit nonlinear canceler operating at a data rate of 2.5 Gb/s.

#### V. SUMMARY AND CONCLUSIONS

In this paper, we have proposed techniques for adaptive nonlinear cancellation of intersymbol interference in the electrical signal at the receiver in Gb/s lightwave systems, and described several demonstrations of these techniques. We first discussed techniques for adjustable nonlinear cancellation, and described demonstrations of these techniques using commercially-available IC's at data rates as high as 1.7 Gb/s. We then discussed techniques for automatic adjustment and described a demonstration of adaptive nonlinear cancellation at 450 Mb/s. Our experimental results showed that these techniques allow reliable detection even when the received signal eye is closed by intersymbol interference, such as from polarization or chromatic dispersion. Finally, we discussed how these techniques can be integrated onto the detector IC for operation at 2.5 Gb/s and higher data rates. These techniques allow a single IC detector with adaptive nonlinear cancellation to be used in future long-haul and undersea lightwave systems (and in present systems as a replacement for the detector IC)

to optimize the detector threshold and compensate for the ISI due to such impairments as polarization and chromatic dispersion, nonideal receiver frequency characteristics, and transmitter/receiver mismatch.

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